Abstracts

Parasitic resistance extraction errors with implications for FET model accuracy around V/sub ds/=0

V.I. Cojocaru and T.J. Brazil. "Parasitic resistance extraction errors with implications for FET model accuracy around V/sub ds/=0." 1997 MTT-S International Microwave Symposium Digest 3. (1997 Vol. III [MWSYM]): 1599-1602.

The accuracy of non-linear FET models around the origin in the V/sub gs/-V/sub ds/ bias plane, may be seriously affected by errors in the extracted values of the source and drain parasitic resistances. In this paper we present test results that prove how relatively small errors of this kind, which can be easily encountered when using conventional extraction techniques, can lead to large errors in the values extracted for some intrinsic parameters, and in particular for the two gate capacitances. The source of these errors is investigated and, as a solution, an improved extraction methodology is offered, which substantially reduces the risk of such errors.

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